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(54) Copper interconnection structure incorporating a metal seed layer

(57) The present invention discloses an interconnection structure for providing electrical communication with an electronic device which includes a body that is formed substantially of copper and a seed layer of either a copper alloy or a metal that does not contain copper sandwiched between the copper conductor body and the electronic device for improving the electromigration resistance, the adhesion property and other surface properties of the interconnection structure. The present invention also discloses methods for forming an interconnection structure for providing electrical connections to an electronic device by first depositing a seed layer of copper alloy or other metal that does not contain copper on an electronic device, and then forming a copper conductor body on the seed layer intimately bonding to the layer such that electromigration resistance, adhesion and other surface properties of the interconnection structure are improved.

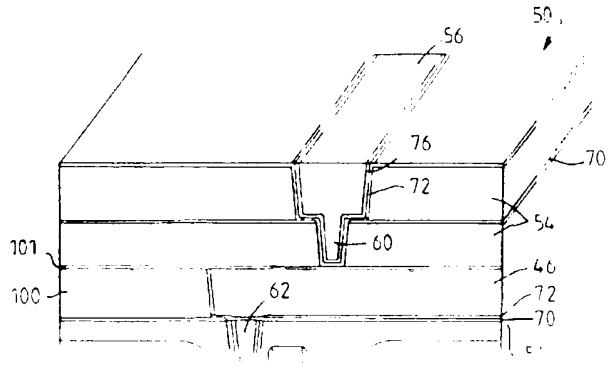

FIG. 2

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Description

Field of the Invention

[0001] The present invention generally relates to an interconnection structure for providing electrical communication with an electronic device, and method for fabricating such structure and more particularly, relates to an interconnection structure for providing electrical connections to an electronic device by the incorporation of a copper alloy seed layer sandwiched in between a copper conductor body and an electronic device for improving the electromigration resistance, the adhesion and the surface properties of the interconnection structure.

Background of the Invention

[0002] The technology of making interconnections to provide for vias, lines and other recesses in semiconductor chip structures, flat panel displays, and package applications has been developed for many years. For instance, in developing interconnection technology for very-large-scale-integrated (VLSI) structures, aluminum has been utilized as the primary metal source for contacts and interconnects in semiconductor regions or devices located on a single substrate. Aluminum has been the material of choice because of its low cost, good ohmic contact and high conductivity. However, pure aluminum thin-film conductors have undesirable properties such as a low melting point which limits its use to low temperature processing, possible diffusion into the silicon during annealing which leads to contact and junction failure, and electromigration. Consequently, a number of aluminum alloys have been developed which provided advances over pure aluminum. For instance, U.S. Patent No. 4,566,177 discloses a conductive layer of an alloy of aluminum containing up to 3% by weight of silicon, copper, nickel, chromium and manganese was developed to improve electromigration resistance. U.S. Patent No. 3,631,304 discloses aluminum alloys with aluminum oxide which were also used to improve electromigration resistance.

[0003] Recently developed ULSI technology has placed more stringent demands on the wiring requirements due to the extremely high circuit densities and faster operating speeds required of such devices. This leads to higher current densities in increasingly smaller conductor lines. As a result, higher conductance wiring is desired which requires either larger cross-section wires for aluminum alloy conductors or a different wiring material that has a higher conductance. The obvious choice in the industry is to develop the latter using pure copper for its desirable high conductivity. However, copper is known to have problems at semiconductor device junctions due to its low electromigration resistance. The electromigration phenomenon occurs when the superposition of an electric field onto random thermal diffusion in a metallic solid causes a net drift of ions in the direction of the electron flow. Any diffusion of copper ions into the silicon substrate can cause device failure. In addition, pure copper does not adhere well to oxygen containing dielectrics such as silicon dioxide and polyamide. To fully utilize copper in interconnection technology, the adhesion properties of copper must also be improved.

[0005] U.S. Patent No. 5,130,274, assigned to the common assignee of the present invention, discloses the use of a copper alloy containing an alloying element of less than 2 atomic % by first depositing an alloy into the recess of an interconnection structure and then forming a copper alloy plug and a thin layer of an oxide of the alloying element on the exposed surface of the plug. However, the technique still does not satisfy the more stringent requirements in ULSI structures where critical dimensions of less than 0.5 μm place a considerable burden on thin film chip interconnections. The use of standard Al (Cu) alloy and a silicon dioxide dielectric in a deep-submicron logic circuit wiring structure results in a large circuit delay caused mainly by the wiring connections.

[0006] The use of Cu as an alternative material to Al (Cu) in ULSI wiring structures to increase the chip speed has been attempted by others. However, numerous problems are incurred in Cu interconnections such as the tendency of Cu to corrode and the fast surface diffusion rates of copper in thin films. It is known that pure Cu has a smaller electromigration activation energy, i. e., 0.5~0.8 ev, than that in Al (Cu) of 0.8~0.9 eV. This implies that the advantage of using Cu for reducing interconnection electromigration failure at chip operating conditions is largely compromised.

[0007] A schematic of an enlarged, cross-sectional view of an electronic structure that utilizes conventional interconnections made of copper alloy is shown in Figure 1. The electronic structure 10 contains two levels of copper interconnections 12, 16 and one stud level 14 illustrating a copper wiring structure by a Damascene process on a prefabricated device 20. The device 20 is built on a semi-conducting substrate 24. As shown in Figure 1, a typical Damascene level is first fabricated by the deposition of a planar dielectric stack 26. The dielectric stack 26 is then patterned and etched using standard lithographic and dry etch techniques to produce a desired wiring or via pattern. The process is then followed by the metal depositions of a thin adhesion/diffusion liner 18 and copper alloy metallurgy 12 wherein a bottom silicon nitride layer 28 is used as a diffusion

the next level copper interconnection 14. After a second level dielectric stack 34 is deposited, a recess for an interconnect is etched into the dielectric layer 34 and the silicon nitride layer 32.

[0008] A interlevel copper alloy stud 14 with liner 22 is then deposited by a technique similar to that used in depositing the first level copper alloy interconnection 12. A variety of metal deposition techniques can be used for filling the trench or via. These techniques include a collimated sputtering process, an ion cluster beam process, an electron cyclotron resonance process, a chemical vapour deposition process, an electroless plating process and an electrolytic plating process. Other techniques such as a co-deposition method in which copper and an alloying element are co-deposited can also be used in forming the copper alloys. For instance, such co-deposition methods include co-sputtering, co-plating, co-chemical vapour deposition and co-evaporation. After the completion of the interlevel copper alloy stud 14, another similar process is repeated to form the second level copper interconnection 16 with liner 24 in a third dielectric stack layer 38. An etch stop layer 36 of silicon nitride is utilized between the stud and the second level interconnections. Finally, a top silicon nitride layer 42 is deposited on top of the copper wiring structure 10 for protecting the device from the environment.

[0009] Other workers have attempted to use copper alloys in providing enhanced electromigration resistance. For instance, U.S. Patent No. 5,023,698 teaches copper alloys containing at least one alloying element selected from the group of Al, Be, Cr, Fe, Mg, Ni, Si, Sn and Zn. U.S. Patent No. 5,077,005 teaches copper alloys containing at least one member selected from In, Cd, Sb, Bi, Ti, Ag, Sn, Pb, Zr and Hf where the weight percent of the alloying element used is between 0.0003 to 0.01. The copper alloys are used in TAB processes and as print circuit board members. U.S. Patent No. 5,004,520 also teaches copper foil for film carrier application containing at least one alloying element selected from P, Al, Cd, Fe, Mg, Ni, Sn, Ag, Hf, Zn, B, As, Co, In, Mn, Si, Te, Cr and Zn with the alloying element concentrations from 0.03 to 0.5 weight percent. The alloys are used as connecting leads in integrated circuit chip mounting. Furthermore, U.S. Patent No. 4,749,548 teaches copper alloys containing at least one alloying element selected from Cr, Zr, Li, P, Mg, Si, Al, Zn, Mn, Ni, Sn, Ti, Be, Fe, Co, Y, Ce, La, Nb, W, V, Ta, B, Hf, Mo and C. The alloying elements are used to increase the strength of the copper alloy. U.S. Patent Nos. 5,243,222 and 5,130,274 teach copper alloys for improved adhesion and formation of diffusion barriers. However, none of these prior work teaches copper alloys that are sufficiently improved for use in ULSI on-chip or off-chip wiring interconnections to meet the electromigration resistratios higher than 1.

[0010] It is therefore an object of the present invention to provide an interconnection structure of copper alloy that does not have the drawbacks and shortcomings of conventional copper interconnection structures.

[0011] It is another object of the present invention to provide an interconnection structure of a copper alloy that has improved electromigration resistance, adhesion properties and other surface properties.

[0012] It is a further object of the present invention to provide an interconnection structure of copper alloy that utilizes a seed layer at the interface between a copper alloy interconnection body and an electronic device it is connected to.

[0013] It is another further object of the present invention to provide an interconnection structure of copper alloy by incorporating a copper alloy seed layer sandwiched in between a copper conductor body and an electronic device to which the interconnection is connected.

[0014] It is still another object of the present invention to provide an interconnection structure of copper alloy by depositing a copper alloy seed layer prior to the formation of the copper conductor body which contains at least one element of Sn, In, C, Ti, Zr, N, O, Cl or S for improving the electromigration resistance of the interconnection structure.

[0015] It is yet another object of the present invention to provide an interconnection structure of copper alloy by depositing a copper alloy seed layer prior to the formation of the copper conductor body which includes at least one element selected from Al, Mg, Be, Ca, Sr, Ba, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, another further object of the present invention to provide an interconnection structure of copper alloy by utilizing a copper alloy seed layer which contains at least one element selected from B, N, P, Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt, Ag, Au, Zn or Cd for improving the surface properties of the interconnection structure.

[0016] It is still another further object of the present invention to provide an interconnection system of copper alloy by depositing a metal seed layer sandwiched between a copper conductor body and an electronic device of a metal selected from Ag, Mo, W or Co to improve the copper conductor deposition process.

[0017] It is still another further object of the present invention to provide a method for forming an interconnection structure by first depositing a copper alloy seed layer on an electronic device and then forming a copper conductor body on the seed layer such that electromigration resistance corrosion resistance and adhesion of the interconnection structure are improved wherein the seed layer includes copper and at least one element selected from the group consisting of Sn, In, Zr, Ti, C, O

Disclosure of the Invention

[0018] According to a first aspect, the present invention provides an interconnection structure for providing electrical connections to an electronic device, as claimed in claim 1.

[0019] Preferably, the copper alloy seed layer comprises copper and at least one element selected from the group consisting of Sn, In, Zr, Ti, C, N, O, Cl and S. the copper alloy seed layer has a thickness between about 0.1 nm and about 100 nm, and further preferably, the copper alloy seed layer has a thickness preferably between about 1 nm and about 100 nm.

[0020] Preferably, the structure further comprising a diffusion barrier layer onto which the copper alloy seed layer is deposited, wherein said diffusion barrier layer is deposited of a material selected from the group consisting of Ta, TaN, W, TaSiN, TiN, WN, WSiN, TiAℓN and TiSiN; wherein said copper alloy seed layer is deposited onto said barrier layer by a technique selected from the group consisting of sputtering, ionized sputtering, chemical vapour deposition, evaporation and electrochemical means.

[0021] Preferably, the body formed substantially of copper is formed by copper and between about 0.001 and about 10 weight percent of at least one alloying element selected from the group consisting of C, N, Cl, O and S.

[0022] Preferably, the copper alloy seed layer is formed of a metal compound, a metal solid solution or a two-phase mixtures of metal phases and the copper alloy seed layer is a copper containing about 0.25 to 1.5 atomic % of Sn or In. The structure is used either on-chip or off-chip.

[0023] Preferably, the structure is a member selected from the group consisting of a via, a line, a stud and a wiring lead for TAB, BGA or PGA, or the structure is a multi-level structure having between 2 and 10 wiring levels, and the structure is built on a previously deposited layer of metal silicide or W stud and W local interconnections.

[0024] Preferably, the copper alloy seed layer comprises copper and at least one element selected from the group consisting of Aℓ, Mg, Be, Ca, Sr, Ba, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Pb, Dy, Ho, Er, Tm, Yb, Lu, Hf, V, Nb, Ta, Cr, Mo, W, Mn, Re, Si and Ge, and wherein said copper alloy seed layer has an electrical resistivity larger than the electrical resistivity for the copper conductor body.

[0025] Preferably, the copper alloy seed layer comprises copper and at least one element selected from the group consisting of B, O, N, P, Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt, Ag, Au, Zn and Cd.

[0026] According to a second aspect the invention of Ag, Mo, W and Co, wherein said metal seed layer having a thickness between about 0.1 nm and about 100 nm. Preferably, further comprising a diffusion barrier layer onto which the metal seed layer is deposited, wherein said diffusion barrier layer is deposited of a material selected from the group consisting of Ti, Ta, Nb, Mo, TaN, W, WN, TiN, TaSiN, WSiN, TiAℓN and TiSiN. Preferably, said structure is used either on-chip or off-chip, said structure is a member selected from the group consisting of a via, a line, a stud and a wiring lead for TAB, BGA or PGA, said structure is a multi-level structure having between 2 and 10 wiring levels.

[0027] According to a third aspect, the invention provides a method for forming an interconnection structure for providing electrical Connection to an electronic device, as claimed in claim 8. Preferably, the copper alloy seed layer comprises copper and at least one element selected from the group consisting of Sn, In, Zr, Ti, C, O, Cl, N and S. The copper alloy seed layer is deposited by a technique selected from the group consisting of reactive or non-reactive sputtering, ionized sputtering, chemical vapour deposition, evaporation and electrochemical means. The copper conductor body is formed by copper and between about 0.001 and about 10 weight percent of at least one alloying element selected from the group consisting of C, N, Cl and O. The copper alloy seed layer is deposited to a thickness between about 0.1 nm and about 100 nm. Further comprising the step of depositing a diffusion barrier layer on said electronic device prior to the deposition step for said copper alloy seed layer. The diffusion barrier layer is deposited of a material selected from the group consisting of Ti, Ta, Nb, Mo, TaN, W, WN, TiN, TaSiN, WSiN, TiAℓN and TiSiN. The interconnection structure is formed in multi-levels having between 2 and 10 wiring levels. In another embodiment, the seed layer comprises copper and at least one element selected from the group consisting of Aℓ, Mg, Be, Ca, Sr, Ba, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, V, Nb, Ta, Cr, Mo, W, Mn, Re, Si and Ge.

[0028] According to a fourth aspect, the invention provides a method as claimed in claim 9. Preferably, the copper alloy seed layer is deposited by a technique selected from the group consisting of sputtering, ionized sputtering, chemical vapour deposition, evaporation and electrochemical means, wherein said copper alloy seed layer is deposited to a thickness between about 0.1 nm and about 100 nm. Further comprising the step of depositing a diffusion barrier layer on said electronic device prior to the deposition step for said copper alloy seed layer, said diffusion barrier layer is deposited of a material selected from the group consisting of Ti, TiN, Ta, Nb, Mo, TaN, W, WN, TaSiN, WSiN, TiAℓN and TiSiN

said metal has an electrical resistivity substantially similar to the electrical resistivity of copper and said metal seed layer having a thickness between about 0.1 nm and about 100 nm.

[0030] In accordance with the present invention, an interconnection structure of copper alloy that has improved electromigration resistance, adhesion properties and other surface properties is provided by utilizing an additional copper alloy seed layer sandwiched between the copper conductor body and the electronic device.

[0031] In a preferred embodiment, an interconnection system for providing electrical connection to an electronic device is provided which includes a copper conductor body and a copper alloy seed layer sandwiched in between and in intimate contact with the copper conductor body and the electronic device for improving the surface properties of the electronic device, the copper alloy seed layer consists of copper and at least one element of B, O, N, P, Fe, Ru, Os, Co, Rh, Ir.connection system for providing electrical communication with an electronic device is provided which includes a copper conductor body and a metal seed layer sandwiched in between and in intimate contact with the copper conductor body and the electronic device for improving the copper conductor deposition process, the metal seed layer is deposited of a metal which has a solubility in copper so low such that substantially no copper compounds can be formed. In general, the metal has an electrical resistivity substantially similar to the electrical resistivity of copper. A suitable metal for the metal seed layer is Ag, Mo, W or Co.

Brief Description of the Drawings

[0032] These and other objects, features and advantages of the present invention will become apparent from the following detailed description and the appended drawings in which:

Figure 1 is an enlarged, cross-sectional view of a conventional interconnection system utilizing copper alloy.

Figure 2 is an enlarged, perspective view of an electronic structure having the present invention interconnection system built therein.

Figure 3A is an enlarged, cross-sectional view of an opening for forming a present invention interconnection system having a diffusion barrier layer deposited therein.

Figure 3B is an enlarged, cross-sectional view of the opening for forming the present invention interconnection system of Figure 3A having a copper alloy seed layer deposited on top of the diffusion barrier layer.

Figure 3C is an enlarged, cross-sectional view of the opening for forming the present invention interconnection system of Figure 3B having a copper conductor material deposited therein.

Figure 3D is an enlarged, cross-sectional view of the present invention interconnection system of Figure 3C having the excess copper removed.

Figure 4A is an enlarged, cross-sectional view of an opening for forming the present invention interconnection system of a dual-Damascene structure having a diffusion barrier layer deposited therein.

Figure 4B is an enlarged, cross-sectional view of the opening for forming the present invention interconnection structure of Figure 4A having a copper alloy seed layer deposited on top of the diffusion barrier layer.

Figure 4C is an enlarged, cross-sectional view of the opening for forming the present invention interconnection structure of Figure 4B having a copper alloy deposited therein.

Figure 4D is an enlarged, cross-sectional view of the present invention interconnection structure of Figure 4C having the excess copper removed.

Detailed Description of the Preferred Embodiments

[0033] The present invention provides a novel interconnection structure for establishing electrical communication to an electronic device by utilizing a copper conductor body and a copper alloy seed layer sandwiched between the conductor body and the electronic device such that the electromigration resistance, the adhesion property and other surface properties are improved. The present invention also discloses an interconnection structure for providing electrical connection to an electronic device by utilizing a copper conductor body and a metal seed layer sandwiched between the conductor body and the electronic device for improving the copper conductor deposition process in which the metal seed layer is deposited of a material of Ag, Mo, W or Co.

[0034] The present invention further discloses a novel method for forming an interconnection structure for providing electrical communication with an electronic device that has improved adhesion with the device by first depositing a copper alloy seed layer onto the electronic device prior to the formation of a copper conductor body on top of the seed layer. The seed layer can be formed by copper and at least one element of Aℓ, Mg, Be, Ca, Sr, Ba, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho,

seed layer deposited by a copper and at least one alloying element of Sn, In, Zr, Ti, C, O, N, Cl or S. Another similar method for forming a conductor for providing electrical communication with an electronic device that has improved surface properties on the electronic device is provided by utilizing a copper alloy seed layer consisting of copper and at least one element of B, O, N, P, Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt, Ag, Au, Zn or Cd. The present invention novel method for forming a conductor to provide electrifurther carried out by utilizing a seed layer that does not contain copper, i.e., a metal seed layer that is deposited of a metal having a solubility and an affinity with copper so low such that no copper compound can be formed, for instance, a metal of Ag, Mo, W or Co.

[0035] Referring now to Figure 2, wherein an enlarged, perspective view of a present invention interconnection structure 50 is shown. The interconnection structure 50 is built on a substrate 52 which may be silicon or other semiconductor material in which electronic devices are contained. The device 66 with W studs and local interconnections 62 are built on a semiconducting substrate 52. Vertical connections between wiring levels are provided by Cu stud structure 60 and W stud structure 62 which connect the wiring to the device contact 64. The device 66 shown generally represents a CMOS transistor, but may be any electronic device.

[0036] To prevent diffusion of copper into the insulators 54 or device 66, diffusion/adhesion barrier layers are normally used to surround the copper 46, 60, and 56. The diffusion/adhesion barrier layers may be insulating layers 70 or conducting layers 72. The conducting diffusion barrier layer 72 also provides adhesion for the copper to the underlying materials, even though they are referred to as simply in this document as the barrier layer. Also shown in Figure 2, are the seed layers 76 and 78 which are normally deposited under the main copper conductor layers 46, 60 and 56. The locations and functions of the seed layers are described in reference to two methods of fabricating the interconnection structures, i.e., a single Damascene process and a dual Damascene process.

[0037] A single Damascene process for fabricating the present invention novel interconnection structure is shown in Figures 3A-3D. In Figure 3A, the structure of a line or stud 46 is shown. An insulator layer 100 and a diffusion/adhesion barrier layer 101 is first deposited and patternee omitted. The liner layer 72 is deposited on top of a nitride etch stop layer 101. This is a fabrication method known as a single Damascene process. Next, a seed layer 78 is deposited over the barrier layer 72, as shown in Figure 3B. The material used for the seed layer and its deposition method are given in a latter section since different materials may be preferred for ductor layer 82 is deposited on top of the seed layer 78. To complete the wiring step in the single Damascene process, the excess copper is planarized by a method such as chemical mechanical polishing such that the excess top surface main conductor 82, seed layer 78 and barrier layer 72 are removed, while leaving an isolated stud or line 46. Finally, an insulator barrier layer is deposited as shown in Figure 3D. This same procedure can be repeated for the next wiring level and/or studs to build a multi-level interconnection structure.

[0039] In a second method of fabricating the present invention novel interconnection system, commonly known as a dual-Damascene process, both a stud and a line level are fabricated in the same process step, for instance, as shown in Figure 2, the line level 56 and the stud 60. Referring now to Figure 4A wherein a barrier layer 72 is first deposited into a combined line/stud opening 84. In the next step of the process, a seed layer 76 is deposited on top of the barrier layer 72, as shown in Figure 4B. A main conductor layer 90 is then deposited to fill the line/stud opening 84. This is shown in Figure 4C. A planarization step, by a technique such as chemical mechanical polishing is then carried out to complete the wiring structure of line 56 and stud 60 together. It should be noted that, in this dual-Damascene process, a silicon nitride etch stop layer 70 is used both in forming the line 56 and the stud 60, or can be omitted. A final passivation and etch stop layer silicon nitride layer 101 is deposited, as shown in Figure 4D.

[0040] The seed layer utilized by the present invention novel interconnection structure serves several desirable functions. For instance, in a chemical vapour deposition process for a main copper conductor, a seed layer is desirable for the initiation of chemical reactions which lead to the deposition of copper. For an electro-plating process for forming a main copper conductor, a seed layer is desirable to provide electrical continuity to the electrodes which supply the plating current. For a high temperature reflow sputtering or chemical vapour deposition process for a main copper conductor, a thin layer is desirable for providing a surface with good wetting and nucleation growth characteristics.

[0041] The main copper conductor body is typically formed not of pure copper, but of a mixture of copper with an alloying element such as C, N, O, Cl or S which have been shown to improve the reliability of the copper conductor, or an alloy of copper with other metals which have also been shown to improve the reliability. The above alloying element in the alloy may be in the range from about .001wt.% to about 10 wt.%.

[0042] The present invention novel seed layer for depositing a copper conductor body can be formed of a copper alloy or other metals that does not contain copper. By the appropriate selection of the alloy seed layer

structure of a seed layer do not have to be the same as the composition and structure of the main conductor copper body. For instance, the seed layer may be an alloy with a higher electrical resistivity than the main conductor copper. Furthermore, the seed layer alloy may not even contain copper. As long as the cross-sectional area occupied by the seed layer is a small fraction of the entire conductor cross-sectional area, the overall line resistance will be determined by the resistivity of the main conductor and thus, not increased undesirably by the seed layer. It should also be noted that the current "metal alloy" used in this application includes metal compounds, as well as solid solutions or two-phase mixtures of metal phases.

[0043] The present invention novel seed layer can therefore be chosen to provide improved electromigration resistance, improved adhesion to the underlying diffusion barrier layer, and improved surface properties suitable for deposition of the main conductor copper body. The novel compositions of copper alloys which have been shown to improve the electromigration resistance relative to pure copper include Cu (Sn), Cu (In), Cu (Zr), Cu (Ti) and Cu (C, N, O, Cl, S). The present invention novel interconnection structure also utilizes copper alloys as seed layers which improve the adhesion properties relative to pure copper which include Cu (Aℓ), Cu (Mg), and alloys of Cu with other reactive metals such as Be, Ca, Sr, Ba, Sc, Y, La, and rare earth series elements of Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu, and Hf, V, Mb, Ta, Cr, Mo, W, Mn, Re, Si and Ge.

[0044] The present invention novel interconnection structure further utilizes additional alloying elements which improve surface properties for the seed layer including B, O, N, P, Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt, Ag, Au, Zn and Cd. It has been found that copper alloys which provide a surface suitable for deposition of the main conductor copper body include those which do not form an excessive amount of surface oxide. Therefore, the alloy seed layer may be formed from copper together with one or more of the above alloying elements in order to obtain the best combination of electromigration resistance, adhesion and surface properties. A typical example of the present invention is a copper alloy with 0.25 to 1.5 atomic % Sn or In. The electromigration life time of Cu (Sn) or Cu (In) greatly exceeds that of pure Cu. It is also possible to interdiffuse Cu, Sn or In, and to cumulate Sn or In at the Cu surface in the temperature range of 300-450°C.

[0045] In a second preferred embodiment of the present invention novel interconnection structure, a metal alloy seed layer which does not contain copper can be advantageously used. The properties of the metal alloy seed layer must meet the requirements of seed-solubility in Cu and forms no Cu compounds. In addition, Ag has low resistivity that is comparable to the main copper conductor. Other metals and alloys of some metals which have low solubility in Cu and form no copper compounds which can be advantageously used in the present invention second preferred embodiment include Mo, W and Co.

[0046] In a third preferred embodiment of the present invention novel interconnection structure, a seed layer that is the same layer as the barrier layer may also be utilized. The properties of the seed layer must meet the requirements of adequate adhesion and diffusion barrier effectiveness plus providing the seeding properties of the normally separated seed layer.

[0047] In still another preferred embodiment of the present invention novel interconnection structure, the barrier layer and the seed layer can be structured such that their properties are graded from one interface to the other. For instance, the composition and structure would be optimized for adhesion at the bottom interface by including, for example, reactive metal constituents. In the middle of the barrier/seed layer, the composition and structure are optimized for diffusion barrier effectiveness by including, for example, refractory metal nitrides with amorphous microstructure. At the top surface of the barrier/seed layer, the composition and structure are optimized for seeding and adhesion of the main copper conductor body by including, for example, copper or silver. It should be obtained by either a sequential deposition of layers, or by deposition of a graded composition structure in one deposition process.

[0048] The present invention advantageous alloy seed layer may be fabricated by many different methods. In general, the seed layer will be deposited onto an underlying barrier layer, which may contain materials such as Ti, Nb, Mo, Ta, TaN, W, WN, TiN, TaSiN, WSiN, TiAlN, TiSiN. The seed layer may be deposited by reactive or non-reactive sputtering from a single alloy target or from multiple targets, by ionized sputtering which directs ionized species to the substrate, by chemical vapour deposition, by evaporation, or by electrochemical means. The alloy seed layer may also be deposited by a sequential deposition of copper and the alloying element, which may then be interdiffused by an appropriate heating treatment.

[0049] A suitable thickness for the present invention novel seed layer may range from several monolayers at smaller than 1 nm, i.e., 0.1 nm, up to about 100 nm in submicrometer line widths, or up to about 20% of the line width in wider lines. A preferred range for the thickness is between about 1 nm and about 100 nm.

Example

structure may have a main body conductor dimensions of less than 0.5 μm line width at the lower wiring levels, and less than 1-2 μm at the higher levels. The thickness of the interlevel insulators may be less than 1 μm or more than 1 μm, for instance, typically 0.5~1.5 μm. These insulator materials may typically contain Si and O, and may contain F, may be polymeric material and may be porous. The insulating diffusion barrier layer may be typically between 10 nm and 100 nm thick, and may typically contain Si and N, or may be polymeric materials. The conducting diffusion barrier layer may have a thickness of about 10 nm, or in the range of several nm to 100 nm. It may contain Ta, Ti, W, Nb, Mo, Si, N, Cl, O and may be amorphous or polycrystalline. For example, TaN, TiN or TaSiN may be suitably used.

[0051] The present invention seed layer may be an alloy of Cu with 0.25 to 1.5 atomic % Sn deposited by sputtering from an alloy target. Its thickness may be in the range between about 0.1 nm to about 100 nm, and more preferably between about 1 nm to about 100 nm. The main copper conductor body may be deposited by chemical vapour deposition or by electrochemical means, and may have an overall thickness between about 0.2 μm and about 1.5 μm. After a planarization process is carried out by a chemical mechanical polishing method, the excess copper, seed layer and diffusion/adhesion layers can be removed. The sequence of fabrication in the dual Damascene process is essentially the same as the single Damascene process for the barrier, the seed and the main copper conductor materials, with the exception that both the wiring level and stud level are completed in one process sequence.

[0052] It should be noted that while the present invention has been illustrated in the above example, alloy seed layers for copper interconnections may be advantageously used by any semiconductor structures in advanced chip applications or display applications.

[0053] The present invention discloses an interconnection structure for providing electrical communication with an electronic device which includes a body that is formed substantially of copper and a seed layer of either a copper alloy or a metal that does not contain copper sandwiched between the copper conductor body and the electronic device for improving the electromigration resistance, the adhesion property and other surface properties of the interconnection structure. The present invention also discloses methods for forming an interconnection structure for providing electrical connections to an electronic device by first depositing a seed layer of copper alloy or other metal that does not contain copper on an electronic device, and then forming a copper conductor body on the seed layer intimately bonding to the layer such that electromigration resistance, adhesion and other surface properties of the interconnection

Claims

1. An interconnection structure for providing electrical connections to an electronic device comprising:

   a body formed substantially of copper, and

   a copper alloy seed layer sandwiched in between and in intimate contact with said body and said electronic device for improving electromigration resistance of said interconnection structure.

2. An interconnection structure according to claim 1, wherein said copper alloy seed layer comprises copper and at least one element selected from the group consisting of Sn, In, Zr, Ti, C, N, O, Cl and S.

3. An interconnection structure according to claim 1, wherein said body formed substantially of copper is formed by copper and between about 0.001 and about 10 weight percent of at least one alloying element selected from the group consisting of C, N, Cl, O and S.

4. An interconnection structure according to claim 1, wherein said copper alloy seed layer is formed of a metal compound, a metal solid solution or a two-phase mixtures of metal phases.

5. The interconnection structure of claim 1, wherein said copper alloy seed layer comprises copper and at least one element selected from the group consisting of Aℓ, Mg, Be, Ca, Sr, Ba, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Pb, Dy, Ho, Er, Tm, Yb, Lu, Hf, V, Nb, Ta, Cr, Mo, W, Mn, Re, Si and Ge.

6. An interconnection structure of claim 1, wherein said copper alloy seed layer comprises copper and at least one element selected from the group consisting of B, O, N, P, Fe, Ru, Os, Co, Rh, Ir, Ni, Pd, Pt, Ag, Au, Zn and Cd.

7. An interconnection structure for providing electrical connection to an electronic device comprises:

   a copper conductor body, and

   a metal seed layer sandwiched in between and in intimate contact with said copper conductor body and said electronic device for improving the copper conductor deposition process, said metal seed layer is deposited of a metal which has a solubility in copper so low such that sub-

device comprising the steps of:

depositing a copper alloy seed layer on an electronic device, and

forming a copper conductor body on said copper alloy seed layer intimately bonding to said layer such that electromigration resistance of said interconnection structure is improved.

9. A method for forming a conductor for providing electrical communication with an electronic device comprising the steps of:

depositing a copper alloy seed layer on said electronic device, and

forming a conductor on top of and in intimate contact with said copper alloy seed layer of copper and between about 0.001 and about 10 weight percent of at least one alloying element selected from the group consisting of C, Cl, N, O and S.

10. A method for forming a conductor for providing electrical communication with an electronic device comprising the steps of:

depositing a metal seed layer on top of said electronic device, said metal seed layer is deposited of a metal that has a solubility in and an affinity with copper so low such that no copper compound can be formed, and

forming a copper conductor body on top of and in intimate contact with said metal seed layer.

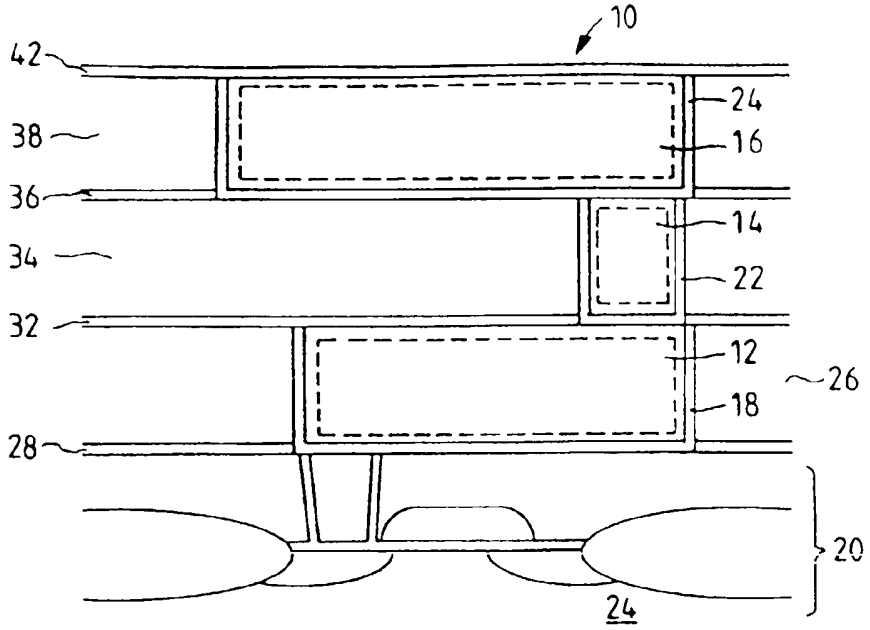
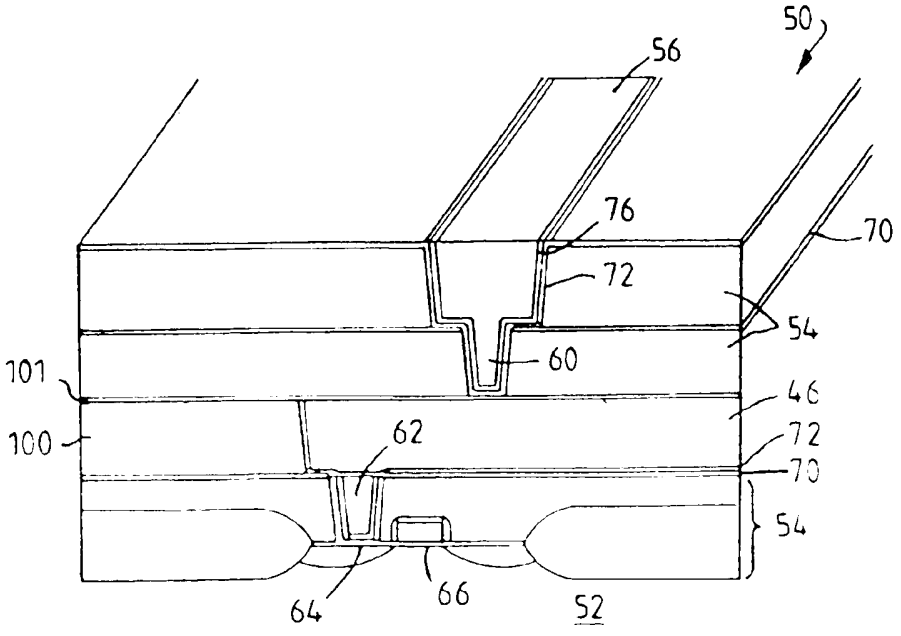


FIG. 1 (PRIOR ART)



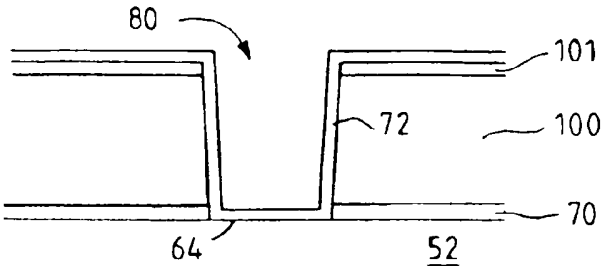


FIG. 3A

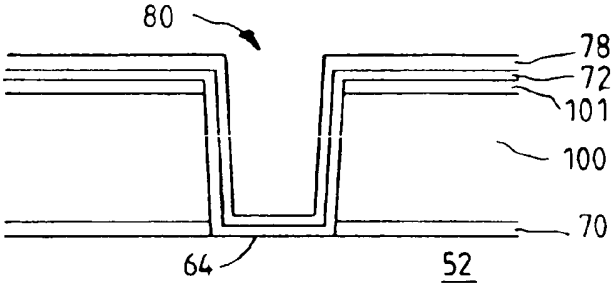


FIG. 3B

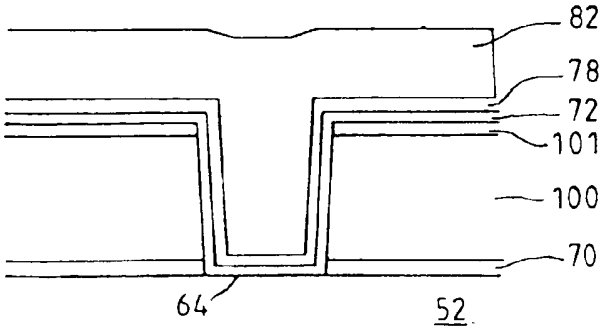
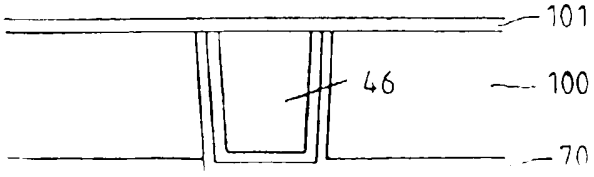


FIG. 3C



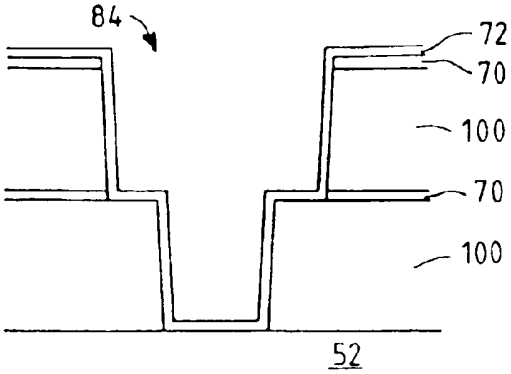


FIG. 4A

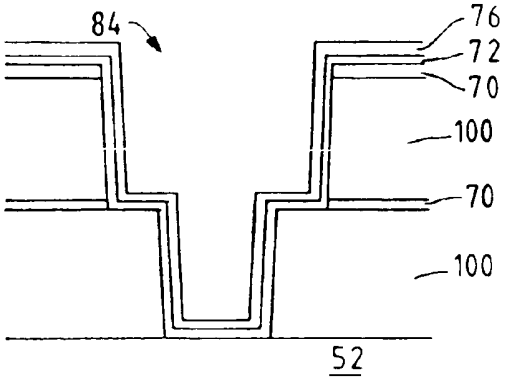


FIG. 4B

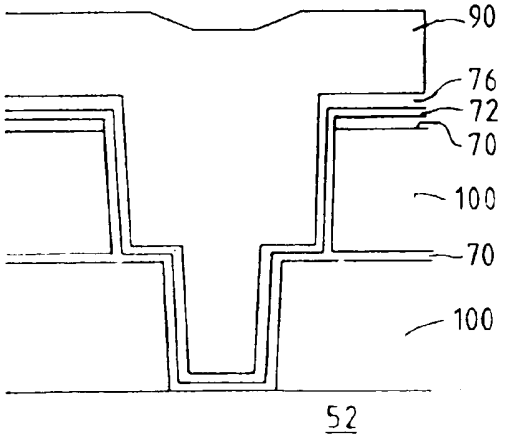
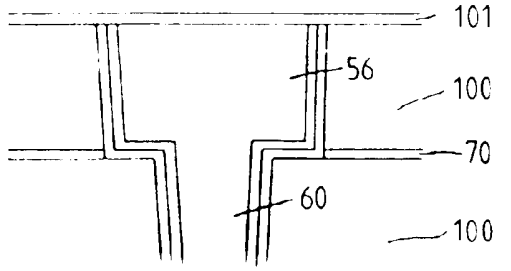


FIG. 4C



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 1767

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	16 August 1999	Munnix, S

CATEGORY OF CITED DOCUMENTS

X particularly relevant if taken alone
Y particularly relevant if combined with another document of the same category

T theory or principle underlying the invention
E earlier patent document, but published on, or after the filing date
D document cited in the application
L document cited for other reasons

European Patent Office

Application Number
EP 99 30 1767

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☒ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 1767

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 097, no. 007, 31 July 1997 (1997-07-31) -& JP 09 069522 A (FUJITSU LTD), 11 March 1997 (1997-03-11) * abstract * * page 6; figures 1-3 *	1,2,6	
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			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	16 August 1999	Munnix, S

CATEGORY OF CITED DOCUMENTS

X particularly relevant if taken alone
Y particularly relevant if combined with another document of the same category
A technological background

T theory or principle underlying the invention
E earlier patent document, but published on, or after the filing date
D document cited in the application
L document cited for other reasons

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LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 99 30 1767

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-6,8-9

Interconnection structure for providing electrical connections to an electronic device, and method for forming such a structure, said structure comprising a body formed substantially of copper and a metal seed layer sandwiched between said body and the electronic device, characterized in that said seed layer is made of a copper alloy.

2. Claims: 7, 10

Interconnection structure for providing electrical connections to an electronic device, and method for forming such a structure, said structure comprising a body formed substantially of copper and a metal seed layer sandwiched between said body and the electronic device, characterized in that said seed layer is made of a metal which forms substantially no compound with copper.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 1767

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report
The members are as contained in the European Patent Office EDP file on
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16-08-1999

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